REMARKS/ARGUMENTS

Drawings

Figure 3a is objected to for reasons stated on page 2 of the Office Action. Figure 3a has been amended to comply with the specification.

Claim Rejections under 35 USC § 103

Claim 1 stands rejected under 35 U.S.C. § 103(a) over Baisuck et al. (US Patent No. 5,299,139) in view of McSherry et al. (U.S. Patent No. 6,230,299). Claims 2-9 stand rejected under 35 U.S.C. § 103(a) over Baisuck et al. (US Patent No. 5,299,139) in view of McSherry et al. and further in view of Heile et al. (US Patent No. 6,321,369). Applicant respectfully traverses the rejections.

When applying 35 U.S.C. § 103, the Examiner is required to adhere to the following tenets of patent law: (1) The claimed invention must be considered as a whole; (2) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination; (3) The references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and (4) Reasonable expectation of success is the standard with which obviousness is determined. (MPEP, 2141.01).

Accordingly, the CAFC in *In re Sang Su Lee* states that the teaching of references can be combined only if there is some suggestion or incentive to do so. *In re Sang Su Lee*, (Fed. Cir. January 18, 2002) (quoting *Acs Hosp. Sys., Inc. v. Montefiore Hosp.*, 732 F.2d 1572, 1577 (Fed. Cir. 1984). Particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed. *Id.* Furthermore, the Court states that even when the level of skill in the art is high, the examiner must explain the reasons one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious. *Id.*

The claimed invention relates to a method for determining location of a short in a circuit. The method contains the steps of running a connectivity extract tool on an artwork of the circuit, determining whether a short exists in the circuit using a short locator tool, and comparing the artwork of the circuit to a schematic of the circuit. The short locator tool may create a copy of the artwork of the circuit and may infer labels to the copy.

Baisuck describes a short-circuit locator method by segregating the area of the electrical node into a plurality of individual polygons. The polygons that represent improper connections are then identified and the short-circuit located.

by determining "success" and "failure", same and different nodes by comparison

McSherry describes a data extraction tool to extract filtered connectivity and geometrical data of an integrated circuit (IC) design. The connectivity and geometrical data for each layout cell hierarchy are extracted at least in part in accordance with specified parasitic effect windows.

Helie describes a method to generate a base design output file in the form of one or more data files including assignment data. A variation design can also be created by adding additional assignments to the assignment data.

As admitted by the Office Action, Baisuck does not teach running a connectivity extract tool on the artwork, nor does it teach comparing the artwork of the circuit to the schematic. Baisuck segregates the area of an electrical node into a plurality of polygons and locates the problem by analyzing contiguous polygons between known reference points. Baisuck locates the short-circuit by tracing the node/polygons multiple times and combining the result of all tracings to identify the problem. Baisuck's operation does not need extraction or copying. Indeed, there are no benefits to performing extraction and copying of the artwork in Baisuck. Accordingly, Applicant respectfully submits that there is no motivation or desirability to extract the connectivity and geometrical data, making a copy of the artwork and inferring labels to the copy of art work. In fact, Basiuck motivates against such a modification and, therefore, one or ordinary skill in the art would not have been motivated to select and combine Basiuck with McSherry and Helie to render the claimed invention obvious. Consequently, these references cannot be combined and claims 1-9 are not rendered obvious.

it does extraction by tracing

Claims 10-17 stand rejected under 35 U.S.C. § 103(a) over Bartels et al. (US Patent No. 6.275,974) in view of Helie. Applicant respectfully traverses this rejection.

Bartels describes a method for tracing a short in a VLSI circuit. The Bartels method does not require a special representation of the design, but only the capability to find all VLSI design component instances intersecting one particular design component instance (Col 2, lines 20-23). Bartels avoids the requirements of extreme storage space and computation time by pruning the shortest path trees with a Breadth First Search (BFS) algorithm so that only the minimum of flat information is stored. In fact, Bartels specifically distinguishes its method by stating that "...**the hierarchical structure of the design**; i.e., components of the design (e.g., an adder or multiplexer), which are used multiple times, **are not copied**; only a 'transform' (an information about what sub-circuit is placed at which coordinates) is maintained." (Col. 3, lines 27-31). As such, Bartels teaches away from examining a schematic of the circuit, creating a copy of the artwork of the circuit, and inferring labels to

the copy of the artwork, as in claim 10. Accordingly, Applicant respectfully submits that Bartels does not suggest the desirability and thus the obviousness of making the combination. Rather, Bartels motivates against the combination. Consequently, Bartels and Helie cannot be combined and claims 10-17 are not rendered obvious.

CONCLUSION

In view of the foregoing remarks, favorable reconsideration of all pending claims is requested. Applicant respectfully submits that this application is in condition for allowance and requests that a notice of allowance be issued. Should the Examiner believe that anything further is required to expedite the prosecution of this application or further clarify the issues, the Examiner is requested to contact Applicant's attorney at the telephone number listed below.

Respectfully submitted,

Dated: **May 1, 2003**

Sean Wooden
Registration No. 43,997
DORSEY & WHITNEY L.L.P.
Suite 400 South
1001 Pennsylvania Avenue, N.W.
Washington, D.C. 20004
Telephone: (202) 442-3000
Fax: (202) 442-3199